PAPER   *Special Section on Analog Circuit Techniques and Related Topics*

A 6 bit, 7 mW, 700 MS/s Subranging ADC Using CDAC and Gate-Weighted Interpolation

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SUMMARY   A 6-bit, 7 mW, 700 MS/s subranging ADC using Capacitive DAC (CDAC) and gate-weighted interpolation fabricated in 90 nm CMOS technology is demonstrated. CDACs are used as a reference selection circuit instead of resistive DACs (RDAC) for reducing settling time and power dissipation. A gate-weighted interpolation scheme is also incorporated to the comparators, to reduce the circuit components, power dissipation and mismatch of conversion stages. By virtue of recent technology scaling, an interpolation can be realized in the saturation region with small error. A digital offset calibration technique using capacitor reduces comparator's offset voltage from 10 mV to 1.5 mV per sigma. Experimental results show that the proposed ADC achieves a SNDR of 34 dB with calibration and FoM is 250 fJ/conv., which is very attractive as an embedded IP for low power SoCs.

key words: *analog-to-digital converter (ADC), Capacitor DAC (CDAC), gate-weighted interpolation, digital offset calibration*

1. Introduction

6 to 7-bit, several hundred MS/s to around 1 GS/s ADCs are required for disk drive front-ends, backplane and ultrawideband receivers. Especially for embedded consumer SoCs, an ultra-low power operation is the most important characteristic rather than high resolution and high speed for the conventional ADC cores. This is because total power reduction is very crucial for portable applications and also for addressing green IT regulation.

Conventionally, the flash architecture has been used for these targets because of an advantage to high speed operation [1]. However, the flash architecture has an essential limitation in reducing conversion energy [2], [3]. An open-loop pipelined ADC has been investigated to attain this target [4], however the power dissipation is still large. The successive approximation register (SAR) architecture has been recognized as the most energy efficient architecture; however, it is not easy to increase the conversion rate up to the GS/s range [5], [6]. An asynchronous SAR ADC with interleaving [7] achieves a relatively high conversion rate but design difficulty is increased. An extremely small FoM of 40 fJ/conv. steps has been attained in a 6-bit 2.2 GS/s ADC using dynamic pipeline architecture [8]. However, this ADC also introduced interleaving technique and the design becomes

complicated.

The subranging architecture is a good solution for this target; however, the results have not been attractive. Although, [9] achieves 1 GS/s conversion rate, the power dissipation is very large due to pre-amplifiers which are introduced to reduce offset voltages. Another subranging ADC [10] achieves 8-bit resolution and 770 MS/s conversion rate; however, large power dissipation by pre-amplifiers and buffers are also problematic. A two-step architecture in [11] shows high resolution, but large power dissipation and low conversion speed reduces its attractiveness.

The work presented here is based on the subranging ADC using the CDAC, gate-weighted interpolation scheme, and digitally offset calibrated double-tail latched comparator [12], [13]. This paper is organized as follows: Sect. 2 introduces the ADC architecture, key schemes and techniques. Section 3 provides the implementation of the proposed ADC. Section 4 details the experimental results, and the paper is finally concluded in Sect. 5.

2. ADC Architecture and Techniques

2.1 Conventional Subranging Architecture

As introduced in Sect. 1, the subranging architecture is an attractive solution for our target specification. However, a conventional subranging architecture has a couple of issues, especially the disadvantage of the power dissipation.

The conventional subranging architecture is shown in Fig. 1 [1]. There are two resistor ladders in the figure. Static current flows through the resistor ladder and this causes large power dissipation. This current can be suppressed by increasing resistance of the resistor ladder. However, reducing the current causes speed degradation, which is not suitable for high speed operation. The pre-amplifiers to reduce comparator's offset are another source of the power dissipation. Furthermore, the buffers for the fine ADC consume static power.

Another issue of the conventional subranging ADC is the conversion precision in the fine ADC. Because the fine ADC decides the resolution of the ADC, it has to have a sufficiently fast settling time and a small offset voltage; therefore, the speed of the ADC is limited. Comparators in the fine ADC also have to satisfy the precision requirement of the ADC in the whole reference range.
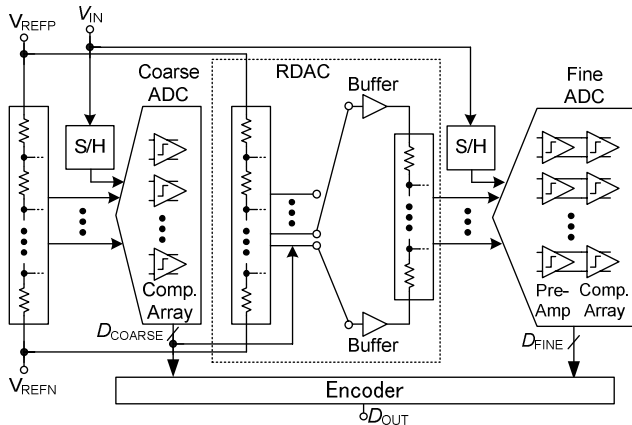
Fig. 1 Conventional subranging architecture.

Fig. 2 Subranging architecture using the CDAC.

Fig. 3 Effect of the input signal reduction in the fine ADC.
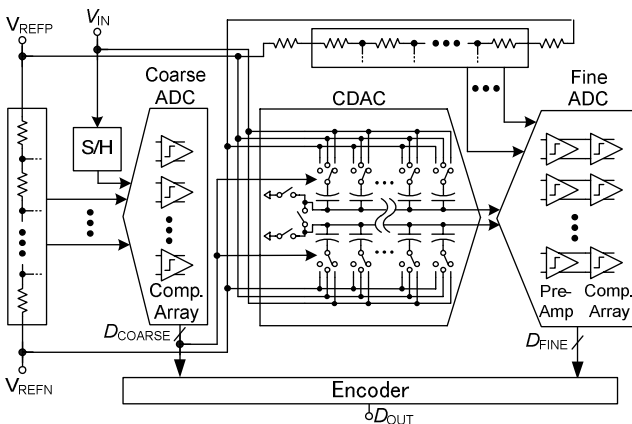
2.2 Subranging ADC Using CDAC

One effective solution to solve the large power dissipation problem in the conventional subranging ADC is to introduce the CDAC for the fine conversion. The subranging architecture using the CDAC is shown in Fig. 2. By introducing the CDAC, S/H and buffers can be eliminated. Also, timing margin for settling is relaxed and fine reference range is fixed around common-mode voltage. However, if there is a parasitic capacitance in the input of the fine ADC such as C_{PI} in Fig. 12, the input signal that is charged into the CDAC is reduced. This affects the ADC's performance. The RMS DNL error, which is caused by the parasitic capacitance, is represented in (1)

$$ERR_{\text{DNL\_RMS}} \text{ [LSB]} = \sqrt{2^{N-1}-1}\left(\frac{1-G_{\text{SIGNAL}}}{G_{\text{SIGNAL}}}\right) \quad (1)$$

where N is a resolution the ADC's and G_{SIGNAL} is the gain of the CDAC. In the fine conversion range, DNL errors occur symmetrically with respect to the midpoint of the range. The amount of the error is represented as $\sqrt{2^{N-1}-1}$ in (1). If there is no parasitic capacitance, G_{SIGNAL} is 1 and $ERR_{\text{DNL\_RMS}}$ becomes 0. However, by increasing parasitic
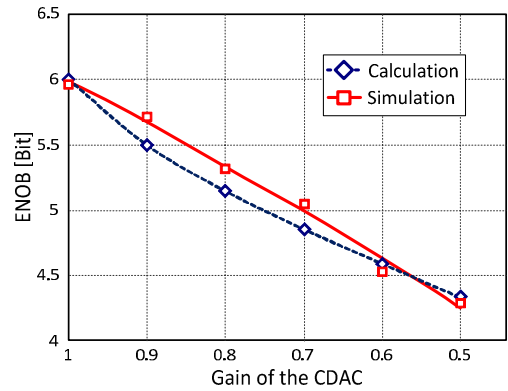
capacitance, G_{SIGNAL} decrease and $ERR_{\text{DNL\_RMS}}$ increases; therefore, the performance of the ADC is degraded.

Figure 3 shows the effect of the signal reduction by the parasitic capacitance in the input of the fine ADC vs. the effective number of bit (ENOB) of the 6-bit subranging ADC. The ideal model is utilized for the simulation. When the parasitic capacitance becomes half of the sampling capacitor, ENOB degrades about 1.7-bit.

The gain degradation problem might be addressed by introducing a gain error adjustment circuit. However, it is not easy to detect the amount of the gain error and guarantee sufficient linearity against PVT fluctuations. Furthermore, additional circuit causes an increase of the power dissipation and core area.

2.3 Proposed ADC Architecture

To solve the previous ADC's issues, we introduced several techniques to our proposed ADC. First, we employ two interleaved fine ADCs to relax the timing margin for the fine conversion. Also, the CDAC is introduced instead of the RDAC to suppress static power dissipation. The gain reduction problem, which is induced by the CDAC and the parasitic capacitance, is solved by the interpolation technique. A gate-weighted interpolation can realize good matching between the coarse and the fine conversion range, even if parasitic capacitances exist in the input of the fine ADC. Digital offset calibration using capacitors reduces the offset voltage of comparators effectively without introducing static power dissipation.

Figure 4 shows the detailed block diagram of the proposed ADC. The coarse ADC consists of reference ladder, S/H, and 4×2-bit interpolation (IP) cells for 4-bit conversion. Each IP cell consists of 4 comparators that use gate-weighted interpolation technique. To realize the interpolation, the coarse ADC requires voltage shifter to generate two differential signal pairs because the input signal of the ADC is only one differential pair. In the coarse ADC, S/H circuit also performs voltage shifting. There is a resistor ladder in the coarse ADC. The total resistance of the resistor ladder is 1.7 kΩ. The resistor ladder consumes 0.3 mW power.

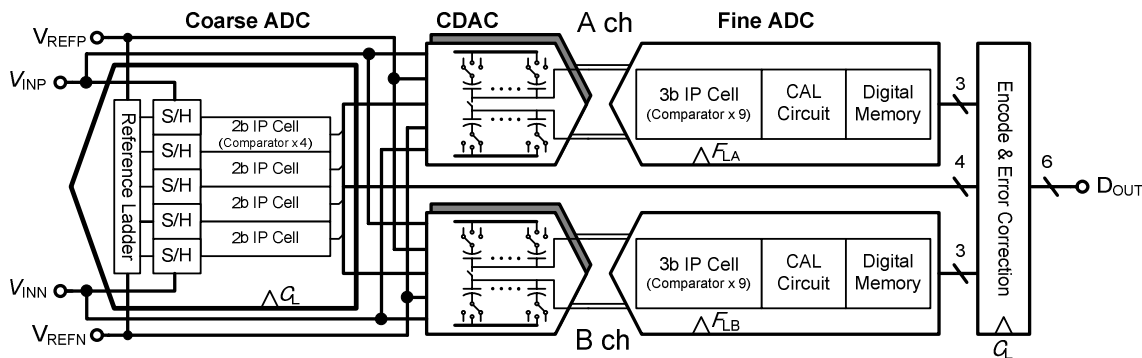Two sets of the CDACs are used in the same way as in
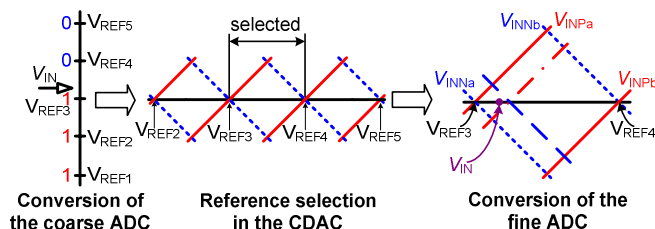
Fig. 4 Proposed subranging ADC architecture.

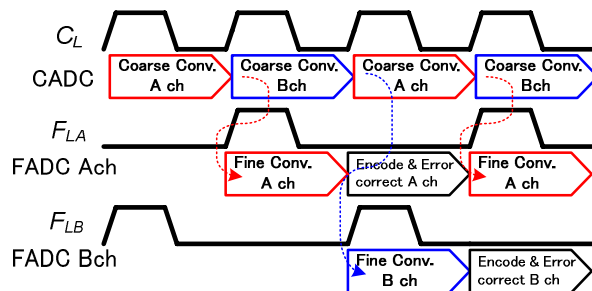
Fig. 5 Conversion process of the proposed ADC.

Fig. 6 Timing chart of the proposed ADC.

[11] to generate voltages for the fine conversion, instead of the conventional resistor ladder, in order to reduce the power dissipation and the settling time, simultaneously. Furthermore, these CDACs act as sample and hold circuits (S/H) like the CDAC in a SAR ADC.

The fine ADC consists of 9 comparators for 3-bit conversion which is illustrated as 3b IP cell in Fig. 4. These comparators mainly determine the resolution of the ADC; therefore, it is necessary to reduce their offset voltages. Digital offset calibration is incorporated to the comparator instead of the conventional method, such as a pre-amplifier, for low power dissipation. In Fig. 4, the CAL circuit and the digital memory blocks mean digital logic circuits and D flip-flops for the offset calibration. Two fine ADCs are interleaved to relax its operating frequency margin. Timing of each ADC is controlled by a clock timing controller. Conversion results from the coarse and the fine ADCs are gathered in digital logics and corrected using one redundancy bit.

Figure 5 shows voltage transfer during conversion of the ADC. When the signal is applied to the ADC, the coarse ADC starts a conversion of 4-bit resolution. After the coarse conversion, two sets of differential signals are outputted from the CDACs for interpolation according to the results of the coarse ADC. Finally, the fine ADC converts the input signal to the digital value in 3-bit resolution using the interpolation. The detailed explanation of the interpolation is shown in Sect. 2.4.

Figure 6 shows a timing chart of the proposed ADC. The coarse ADC operates at the same speed as the sampling frequency; however, the fine ADCs operate at half of the conversion frequency to relax the requirement for the set-

tling time and the timing margins. The fine ADC does not consume any power when it does not convert; therefore, the power dissipation does not increase although the circuit size is increased.

2.4 Interpolation

The proposed ADC addresses the gain reduction issue by using interpolation, which makes it possible to realize fine conversion without any reference voltages and to avoid the effect of the input parasitic capacitance of the fine conversion stages. To implement the interpolation, we introduce a gate-weighted interpolation scheme in the saturation region of MOS transistor to reduce the number of S/H circuits and input capacitance. The circuit implementation is described in Sect. 3.2.

Figure 7 shows the 3-bit interpolation in the fine ADC of the proposed ADC. Two differential outputs from CDAC_a and CDAC_b are used to realize the interpolation. These output signals are shifted by 0.5 coarse LSB to realize one bit redundancy (half over range and half under range) for digital error correction [14].

The interpolated voltages V_{Pi} and V_{Ni} in Fig. 7 can be represented as below

$$V_{Pi} = \frac{\left(2^d - i\right) V_{INPa} + i V_{INPb}}{2^d} \tag{2}$$

$$V_{Ni} = \frac{\left(2^d - i\right) V_{INNa} + i V_{INNb}}{2^d} \tag{3}$$

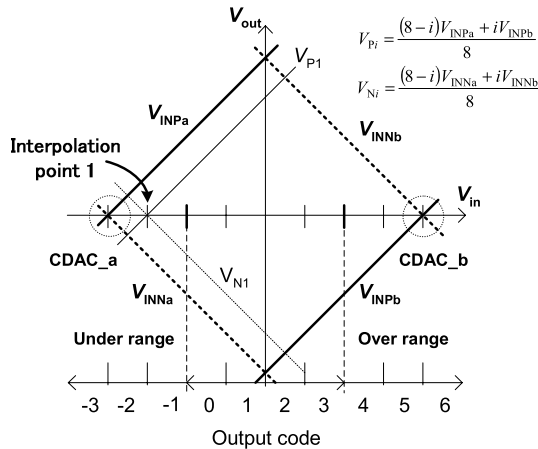where d is a resolution of the interpolation, i is the number of

$$V_{Pi} = \frac{(8-i)V_{INPa} + iV_{INPb}}{8}$$

$$V_{Ni} = \frac{(8-i)V_{INNa} + iV_{INNb}}{8}$$

Fig. 7   Interpolated voltages and output code in fine conversion.

(a) Gain of the CDAC is 1   (b) Gain of the CDAC is 0.5
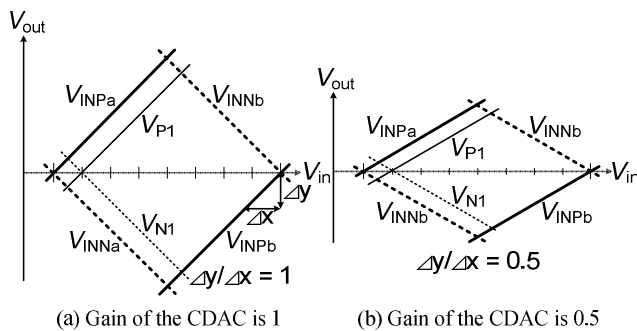
Fig. 8   Mitigation of the gain error by the interpolation.

(a) Conceptual diagram   (b) Concentpual diagram
of the CDAC   of the RDAC

Fig. 9   Conceptual diagram of the CDAC and the RDAC.

Table 1   Component values for analyses.

h	C_U	C_S	C_{PI}	R_{SW}	R_U
16	15 fF	250 fF	50 fF	850 Ω	10 Ω

the interpolated voltage, V_{INPa} and V_{INNa} are the differential output voltages from the CDAC_a and V_{INPb} and V_{INNb} are the differential voltages from the CDAC_b. For example, at the interpolation point 1 (between −2 and −1), conversion is executed by using only V_{P1} and V_{N1}. The other conversions are also realized by the interpolated signals. Therefore, reference voltages are not required for the fine conversion and consistency between the coarse and the fine conversion range is realized automatically.

Figure 8 shows the effect of the gain reduction of the input signal for the fine ADC when using the interpolation. Even though the signal gain is reduced, as long as the reduction ratio of two differential signals is the same, the comparison point does not change. Therefore, the proposed ADC does not require a gain error correction circuit to solve this problem.

2.5   Reference Selection

We utilized the CDAC instead of the RDAC for the proposed ADC. The reason why the CDAC is used is described in this section.

Figure 9 shows the conceptual diagram of the CDAC and the RDAC. Both DACs basically consist of passive elements. The CDAC generates its output voltages using charge distribution of the capacitors and the RDAC gener-
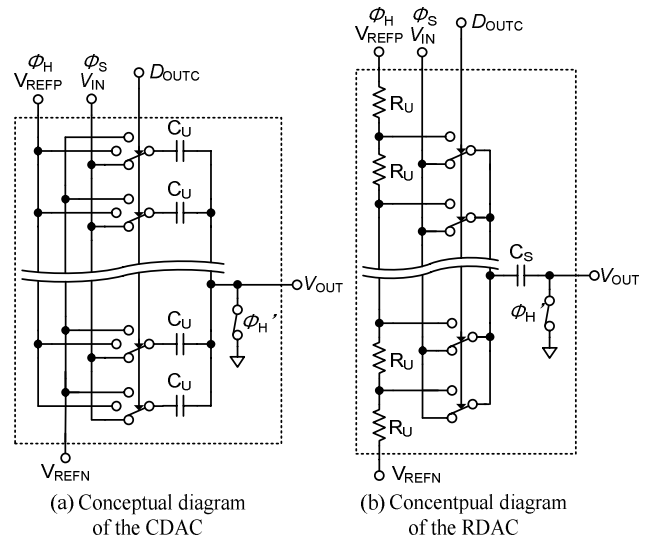
ates its output voltages using voltage division of the resistor ladder.

The CDAC and the RDAC work in a very similar way. For example, during Φ_S (sampling mode), an input signal is charged to the capacitors, all of the unit capacitor, C_U and sampling capacitor, C_S. After that, during Φ_H (holding mode) in the CDAC, one side of capacitors are connected to V_{REFP} or V_{REFN} depending on the results of the coarse conversion, and another side of the capacitors are connected to the input of the fine ADC. In the RDAC, one side of C_S, is connected to a certain node of the resistor ladder by the coarse comparison results. Another side of C_S is connected to the fine ADC in the same way as the CDAC.

To compare the two DACs in detail, the analysis of settling time, power dissipation and noise follows. Table 1 summarizes the components values for the analysis and the simulation. Those values of C_U and R_{SW} came from design parameters of the proposed subranging ADC [13]. In the CDAC, R_{SW} is the resistance of PMOS or NMOS switch in the reference select circuit. In the proposed ADC, the average resistance of PMOS and NMOS switch is about 850 Ω; therefore, R_{SW} is assigned that value. h is the number of unit capacitors (resistors). The total number of switches in both of the two DACs is 16, which is the same value as h. For the RDAC, C_S is the sum of C_U and R_{SW} is same as the CDAC. C_{PI} is parasitic capacitance of the subsequent circuit, such as the fine ADC. The value of C_{PI} is assumed to be 50 fF which is estimated from the proposed fine ADC [13].

In the RDAC, another resistive component R_U exists. Basically, the value of R_U is decided for the optimal power dissipation and settling time with consideration of R_{SW}.
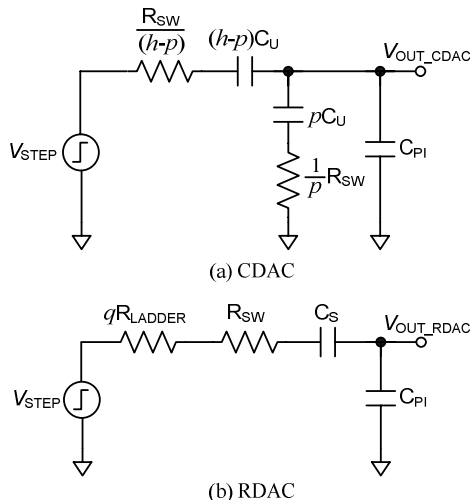
(a) CDAC

(b) RDAC

Fig. 10   Circuit models for settling time analysis during holding mode.

Fig. 11   Simulation results of settling time.

(a) CDAC

(b) RDAC

Fig. 12   Power dissipation during holding mode.

However, in this comparison, R_{SW} is decided first by the CDAC. When using that value of R_{SW}, even if R_U is set to $0\,\Omega$, the RDAC shows slower settling time than the CDAC. Although R_U cannot influence the following comparison of the settling time, it affects the power dissipation and also settling time a little.

In this comparison, R_U is assigned to $10\,\Omega$. For values less than $10\,\Omega$, the power dissipation of the RDAC increases drastically, but the settling time is only reduced by about 5 ps. More detail data is shown in Sect. 2.5.2

2.5.1   Settling Time

To calculate settling time, we use the simplified models of the CDAC and the RDAC during holding mode. In Fig. 10, p is the number of parallel connection, R_{LADDER} is the sum of resistance of the resistor ladder and q is the variation coefficient by the connected position in the resistor ladder. We ignore parasitic capacitance in each node of the resistor ladder to simplify this analysis.

$$V_{OUT\_CDAC} = V_{STEP}\left(1 - \frac{p}{h}\right)\frac{1}{1 + \frac{C_{PI}}{hC_U}}\left(1 - e^{-\frac{1 + \frac{C_{PI}}{hC_U}}{\frac{R_{SW}}{h}C_{PI}}t}\right) \quad (4)$$

$$V_{OUT\_RDAC} = V_{STEP}\frac{1}{1 + \frac{C_{PI}}{C_S}}\left(1 - e^{-\frac{1 + \frac{C_{PI}}{C_S}}{(qR_{LADDER} + R_{SW})C_{PI}}t}\right) \quad (5)$$

Equations (4) and (5) represent the settling time of the CDAC and the RDAC, respectively. By these formulas, it is recognized that reducing resistance of the switch and the parasitic capacitance is important for faster settling time.

Simulation results are shown in Fig. 11. According to the simulation results, the CDAC shows faster settling. The difference of the settling time between the two DACs is due to the difference of the resistance. In the CDAC, R_{SW} is divided by h. However, in the RDAC, R_{SW} is added with resistance of the resistor ladder.
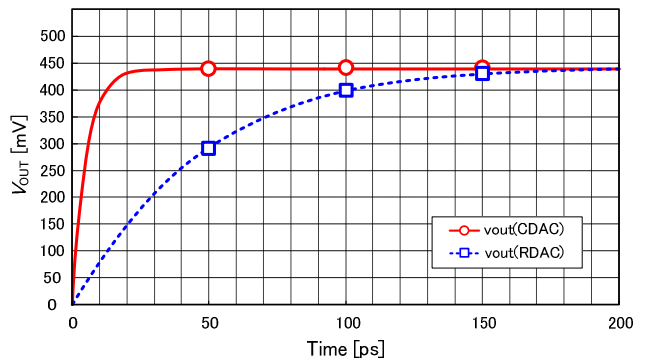
In the RDAC, the settling time can be reduced by using a smaller R_{LADDER}; however, it results in an increase of the power dissipation. Reducing R_{SW} also contributes to faster settling time. However, it increases the parasitic capacitance of the switch; therefore, the settling time and the power dissipation is increased.

2.5.2   Power Dissipation

Figure 12 shows a mechanism of the power dissipation in the CDAC and the RDAC during the holding mode. Assume that the input signal is already charged to C_U and C_S during the sampling mode and no leakage current flows in the DAC circuits.

$$P_{d\_CDAC} = f_{sample}\left(C_{P\_CDAC} + C_{PI}\right)\left(V_{REF} - V_{IN}\right)^2 \quad (6)$$

$$P_{d\_RDAC} = \frac{V_{REF}^2}{R_{LADDER}}$$

$$+ f_{sample}\left(C_{P\_RDAC} + C_{PI}\right)\left(V_{REF\_N} - V_{IN}\right)^2 \quad (7)$$

Equations (6) and (7) represent the power dissipation in the CDAC and the RDAC respectively. f_{sample} means sampling frequency of the ADC and in (7), V_{REF_N} is N-th reference voltage in the resistor ladder. Equation (6) indicates
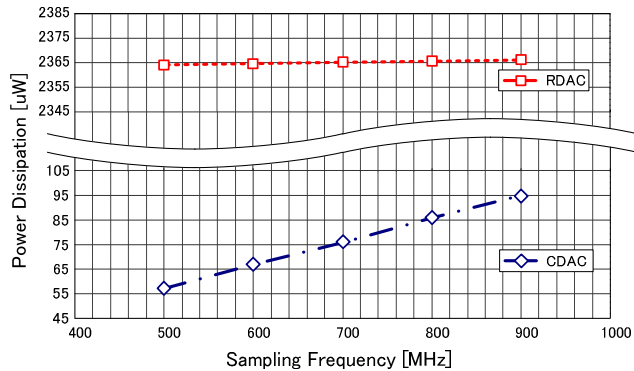
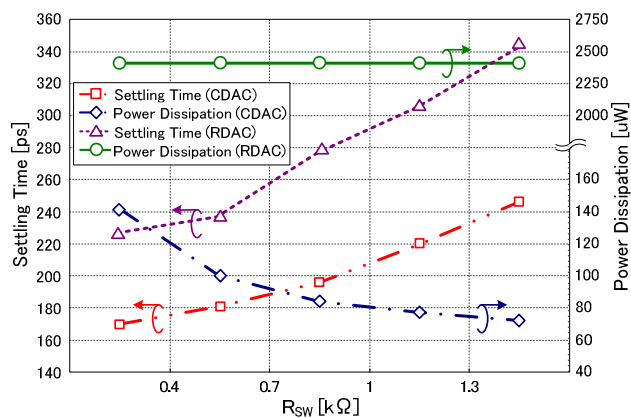**Fig. 13** Simulation results of power dissipation vs. sampling frequency.

Fig. 14 Simulation results of power dissipation and settling time vs. R_{SW}.

Fig. 15 Simulation results of power dissipation and settling time vs. R_U in RDAC.

(a) CDAC in sampling mode   (b) CDAC in holding mode
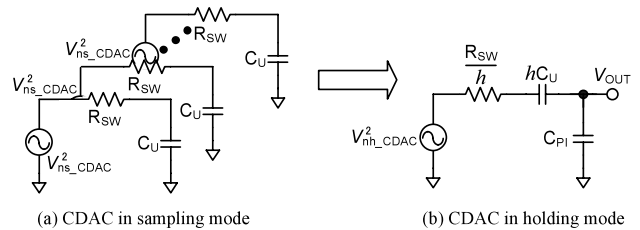
Fig. 16 Circuit model of the CDAC for noise analysis.

that the power dissipation of the CDAC is same as the digital circuit. On the other hand, (7) includes not only dynamic power dissipation but also static power dissipation caused by the resistor ladder.

Figure 13 shows simulation results of the power dissipation vs. sampling frequency. In this simulation condition, the settling times of the CDAC and the RDAC are about 190 ps and 280 ps, respectively. For fair comparison, the settling time should be set to the same. However, as mentioned in Sect. 2.5, adjusting settling time using only R_U is quite difficult. Changing other parameters also affect to the CDAC and causes other issues.

There is a large difference of the power dissipation between two DACs', such as 76 μW vs. 2.4 mW at 700 MHz sampling frequency. The power dissipation of the CDAC is changed with sampling frequency because it works like a digital CMOS circuit. Although the RDAC partially consumes dynamic power, the main source of its power dissipation is static current. Therefore, the power dissipation in the RDAC barely changes with increasing the sampling frequency.

The simulation results of the power dissipation and the settling time vs. R_{SW} are shown in Fig. 14. The CDAC shows faster settling by more than 60 ps under the same R_{SW} condition. The settling times of the CDAC and the RDAC
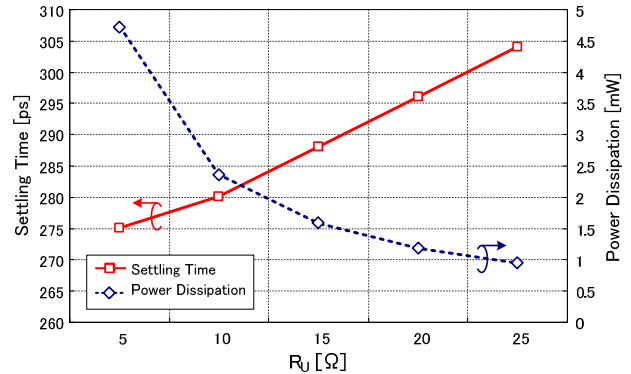
become faster with decreasing R_{SW}; however, power dissipation also increases due to the parasitic capacitance. For the RDAC, the power variation is quite unnoticeable because the power dissipation is dominated by the static current in the resistor ladder.

The effect of R_U to the power dissipation and the settling time in the RDAC is shown in Fig. 15. R_U affects both of the power dissipation and the settling time, especially the power dissipation. However, even if R_U is set to 5 Ω, the RDAC's settling time is still larger than that of the CDAC.

2.5.3 Noise

Contrary to the previous analysis, noise analysis has to consider both the sampling mode and the holding mode. Figure 16 shows the circuit models of the CDAC for noise analysis. During the sampling mode, all of C_U charges noise. During the holding mode, each series connected R_{SW} and C_U is seen as a parallel connection at node V_{OUT}, and the charged noise is distributed to C_{PI}. Finally, adding up the noise during two modes, the total noise is represented in (8).

$$V_{n\_CDAC}^2 = kT \left(\frac{1}{hC_U} + \frac{1}{C_{PI}\left(1 + \frac{C_{PI}}{hC_U}\right)} \right) \tag{8}$$

Noise analysis for the RDAC is simpler than the CDAC since there is only one signal path as shown in Fig. 17. During the sampling and the holding modes, circuits can be simplified to RC network. Calculation result is represented in (9), which is identical to (8) when $h * C_U = C_S$.
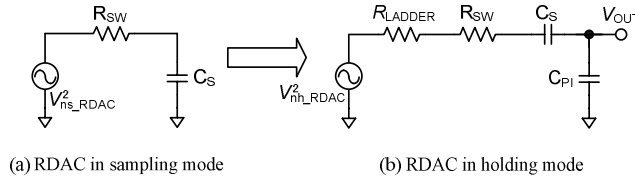
(a) RDAC in sampling mode   (b) RDAC in holding mode

Fig. 17   Circuit model of the RDAC for noise analysis.

Fig. 18   CDAC with S/H circuit.

$$V_{n\_RDAC}^2 = kT \left(\frac{1}{C_S} + \frac{1}{C_{PI} \left(1 + \frac{C_{PI}}{C_S} \right)} \right) \tag{9}$$

Although the noise calculation results of the CDAC and the RDAC are the same, it has to be considered that the difference of resistance between the two DACs. During the sampling mode, both of the DACs utilize the same switches; this means the charged noise are equal. The difference appears during the holding mode. R_{SW} of the CDAC is divided by h due to its parallel connection. On the other hand, R_{SW} of the RDAC is shown as it is. Moreover, the RDAC incorporates resistor ladder, which is another noise source.

If noise bandwidth is considered to infinity, total noise of the two DACs becomes the same. However, the bandwidth is limited by the subsequent circuit, in this case, comparators in the fine ADC. Therefore, the accurate noise has to be analyzed with the bandwidth limitation by the comparators.

In Sect. 2.5, the CDAC and the RDAC are compared in settling time, power dissipation and noise. Through the above analysis, the CDAC shows better performance than the RDAC around several hundred of operating frequency. Therefore, it is reasonable to incorporate the CDAC for the proposed subranging architecture.

3. ADC Implementation

3.1 CDAC with S&H

The CDAC is composed of 17 unit capacitors (C_U) and one capacitor to make the offset voltage for one bit redundancy as shown in Fig. 18, where one side of circuitry of differential scheme is illustrated. The unit capacitance is 15 fF and it samples and holds the input signal like the CDAC in a SAR ADC. Sampling switches uses bootstrapping technique to reduce the on-resistance and the signal distortion.

When Φ_S goes high, V_{IN} is sampled into the capacitors. Next, Φ_H goes high, capacitors are connected to V_{REFP} or V_{REFN} depending on the results of the coarse conversion. Considering parasitic capacitance C_{PI}, V_{OUT} can be represented as below,

$$V_{OUT} = \frac{C_U \{ (mV_{REFP} + nV_{REFN}) - (m+n) V_{IN} \} + C_{OFS} V_{OFS}}{C_U (m + n) + C_{PI}} \tag{10}$$

where m and n are the number of capacitors which connected to V_{REFP} or V_{REFN}, respectively. C_{OFS} and V_{OFS} mean capacitor and reference voltage to generate offset voltage for one bit redundancy. Equation (10) indicates that C_{PI}
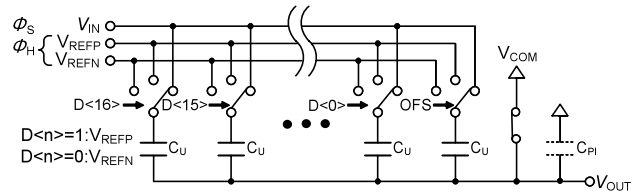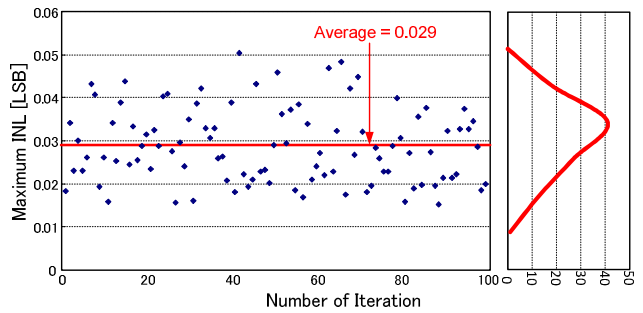

Fig. 19   Simulation results of the maximum INL.

reduces V_{IN} swing range, which causes the issue of the conventional subranging ADC. The proposed ADC addresses this issue by introducing the interpolation.

3.1.1 Mismatch of the CDAC

The size of the unit capacitor has to be set with consideration of the mismatch error. Especially for the CDAC, the DNL error is affected by not only the capacitor mismatch but also the number of the unit capacitors.

The total capacitance of the CDAC is decided by noise of the circuit. Because the total capacitance is fixed, the unit capacitance and the number of capacitors are inversely proportion. Therefore, if the number of unit capacitors increase, the mismatch of the CDAC is also increased. The DNL error calculation result per sigma with consideration of the mismatch and the number of unit capacitors is represented in (11)

$$DNL(\sigma) \, [\text{LSB}] = 2^N \frac{\Delta C_{total}}{C_{total}} (\sigma) \frac{1}{\sqrt{h}} \sqrt{1 - \frac{1}{h}} \tag{11}$$

where N is the resolution of the proposed ADC, C_{total} is the total capacitance of the CDAC, and h is the number of capacitors in the CDAC. When the unit capacitance is decreased, the mismatch of the unit capacitance is increased with $\sqrt{h}$. However, in the CDAC, the output error caused by the mismatch of the unit capacitance is also suppressed by $1/h$, because the signal range is divided by h. Finally, DNL error is reduced by about $1/\sqrt{h}$. The calculation result of $DNL(\sigma)$ is 0.011 LSB and the maximum $INL(\sigma)$ derived from $DNL(\sigma)$ is 0.03 LSB. See Appendix A for more details.

Figure 19 shows the maximum $INL(\sigma)$ simulation results with 100 times iteration. Averaged the maximum $INL(\sigma)$ is 0.0292 LSB, which shows good matching with
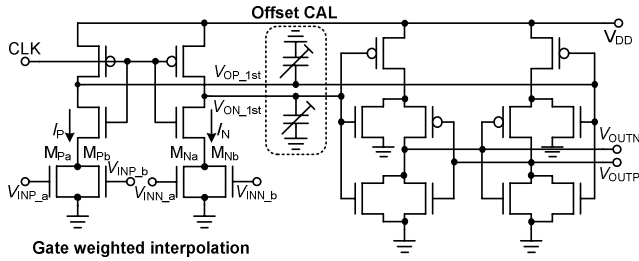
Fig. 20 Double-tail latched comparator with interpolation and offset calibration.

Fig. 21 Simulation results of non-linearity error of MOS transistor.

Fig. 22 Process of the offset voltage calibration.

the calculation. Target specifications of the INL & DNL are less than 0.25 LSB each; therefore, the CDAC satisfies the requirements with plenty of margin.

3.2 Comparator with Gate-Weighted Interpolation

The double-tail latched comparator with gate-weighted interpolation shown in Fig. 20 is employed in the proposed ADC. The comparator consists of 4 input MOS transistors for interpolation. The gate-weighted interpolation technique is very effective to reduce the power consumption. The interpolation method which is incorporated in [15] utilizes the on-conductance of a transistor in the linear region. In contrast, we realized the interpolation in the saturation region.

Drain current in the saturation region of a classical long channel MOS transistor exhibits a square-law relationship to $(V_{gs}-V_T)$ and causes non-linearity error when using an interpolation. However, the drain current of the recent scaled MOS transistor is proportional to $(V_{gs}-V_T)$ due to the heavy velocity saturation effect. The drain current of the input transistor, I_D, can be expressed as

$$I_D \approx \alpha W \left(V_{gs} - V_T{}' \right) \tag{12}$$

where α is a coefficient, W is the gate width, and $V_T{}'$ is the effective threshold voltage. We used the value of 290 mV as the $V_T{}'$.

In Fig. 20, current I_P is the sum of the currents in M_{Pa} and M_{Pb}. Also, I_N is the sum of the currents in M_{Na} and M_{Nb}. The current I_P is represented as below

$$I_P = \alpha \{ W_{Pa} (V_{INP\_a} - V_T{}') + W_{Pb} (V_{INP\_b} - V_T{}') \} \tag{13}$$

where W_{Px} means the gate width of the MOS transistor M_{Px}. Equation (13) shows that I_P can be controlled by changing gate width, W_{Px}, even if the input voltages are not changed. The ratio between W_{Pa} and W_{Pb} is set by the ratio of the interpolation. The I_N is also calculated in the same way. Comparators in each interpolating points compare using each I_P and I_N. This concept is shown in Fig. 7.

The simulation results of the interpolation error using the same size of the input MOS transistor is shown in Fig. 21. The simulated interpolation range is assigned ±100 mV from Vcom voltage. The interpolation error is less than 0.1 LSB when Vcom voltage is higher than 600 mV. Therefore, in those Vcom voltages, the gate-weighted interpolation can be realized with sufficient accuracy. However,
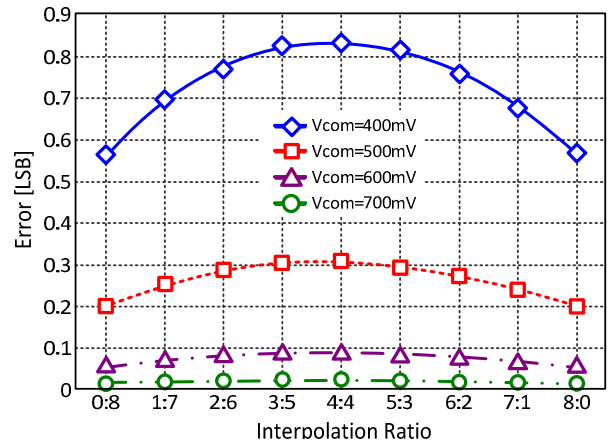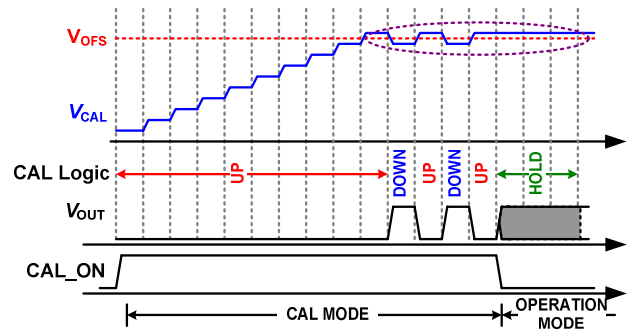
it is difficult to realize the interpolation with Vcom of less than 500 mV, due to the increase of non-linearity.

3.3 Offset Calibration

An offset calibration technique by adjusting capacitance [16] is incorporated to the comparators in the fine ADC. 4-bit binary weighted PMOS varactors are used as voltage controlled capacitors. The gate size of a unit varactor is 200 nm × 100 nm.

Figure 22 shows the calibration process. In Fig. 22, V_{CAL} is the calibration voltage in the calibration logic and V_{OFS} is the offset voltage of the comparator. During calibration mode, all input nodes of the comparator are connected to the common voltage. Since all input nodes are the same, the output is determined by the offset voltage. Therefore, calibration logic changes the calibration code to cancel the offset voltage; as a result, V_{CAL} gets closer to V_{OFS}. When V_{CAL} approaches to V_{OFS} within voltage difference of one bit resolution of calibration, the calibration process is ended. After that, calibration code oscillates around the best calibration result. The comparator incorporates 4-bit calibration that operates at the same frequency as the clock resulting in a merely 16 clock cycles calibration process. The resolution of the calibration logic is about 2 mV, which is small enough for the 1/2 LSB (about 9 mV) of the proposed ADC,. The number of bit for calibration is determined by Monte Carlo

simulation.

The Monte Carlo simulation results show that large mismatch of about $10\,\text{mV}(\sigma)$ can be suppressed to $0.9\,\text{mV}(\sigma)$ with calibration. The propagation delay with calibration at the input drive voltage of 1 mV is 140 ps and consumed energy for one conversion is 63 fJ/conv. The input referred noise voltage is about 0.7 mV per sigma of which value is reduced to 64% for the comparator without offset calibration. The increase of node capacitance reduces input referred noise voltage.

3.3.1 Offset Calibration at each Interpolating Point

The introduced offset calibration technique adjusts the slew rate at the $V_{\text{OP\_1st}}$, $V_{\text{ON\_1st}}$ nodes in Fig. 20. This slew rate is affected by not only capacitance at the nodes of the $V_{\text{OP\_1st}}$ and $V_{\text{ON\_1st}}$ but also by the input common-mode voltage. During the calibration mode, all of the comparators are using the same input common-mode voltage. However, in the operation mode, each comparator has a different interpolating ratio, this also means that the input common-mode voltage of each comparator is different. This results in the difference of slew rate between the calibration mode and the operation mode. Therefore, it is necessary to verify that this offset calibration method is effective to reduce the offset voltage for each interpolating point with different input common-mode voltage.

To examine the effect of input common-mode voltage, we introduced variation of V_{eff} against variation of the capacitance at the output nodes such as $V_{\text{OP\_1st}}$ and $V_{\text{ON\_1st}}$. The result is shown in (14).

$$\frac{\partial V_{off}}{\partial C_{\text{o\_1st}}} = -\frac{V_{eff}}{2C_{\text{o\_1st}}} \tag{14}$$

where V_{off} is the offset of the comparator, V_{eff} is $(V_{\text{gs}}\text{-}V_{\text{t}})$ of the input MOS transistor and $C_{\text{o\_1st}}$ is the capacitance at the output nodes of $V_{\text{OP\_1st}}$ and $V_{\text{ON\_1st}}$. Equation (14) shows the variation of the offset voltage is proportional to V_{eff}; therefore, it is effective to reduce V_{eff} to achieve more accurate offset calibration.

The 1000 times Monte Carlo simulation results of input referred offset voltage after calibration at each interpolating point for 3 common-mode voltages are shown in Fig. 23.
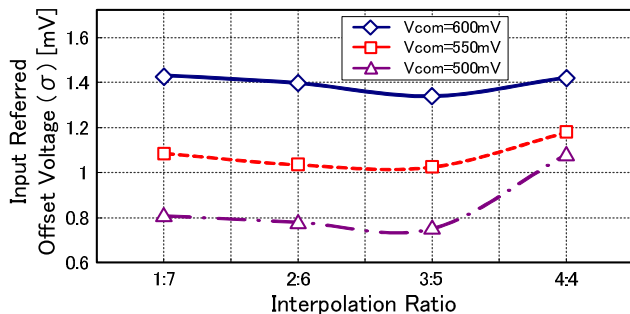

Fig. 23 Input referred offset voltage after calibration at each interpolating point.

The simulation results show that the offset calibration is effective for all interpolation ratios even if the common-mode voltage is changed from 500 mV to 600 mV. This means that the variation of the slew rate is small enough.

4. Experimental Results

The proposed ADC has been fabricated in a 90 nm CMOS technology. Figure 24 shows the chip micro-photograph and the layout of the ADC, which occupies an active area of $0.13\,\text{mm}^2$.

Figure 25 shows the measured DNL and INL at the conversion rate of 700 MS/s after the offset calibration. The DNL is less than ±0.6 LSB and the INL is less than ±0.8 LSB. The DNL/INL results are not as good as our expectation. The most likely reason for the degraded performance is the offset of the comparators in the coarse ADC, which don't incorporate offset calibration logic. If the offset voltage is large enough to affect the accuracy of the coarse ADC, the DNL/INL are degraded. About 16 periodic error patterns in the measurement results support our expectation.

Figure 26 shows the spur free dynamic range (SFDR) and the signal to noise and distortion ratio (SNDR) vs. the sampling rate when the input signal frequency is about 50 MHz. The SNDR maintains higher than 34 dB (5.3 bit) until 700 MS/s and drops down to 20 dB (3.0 bit) at
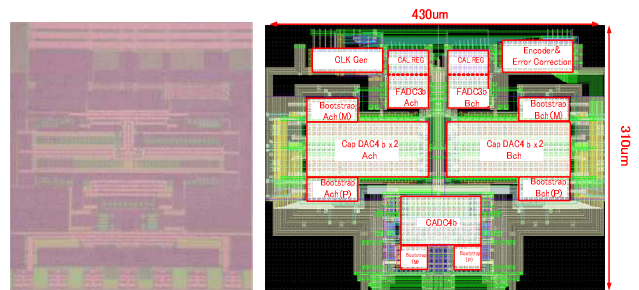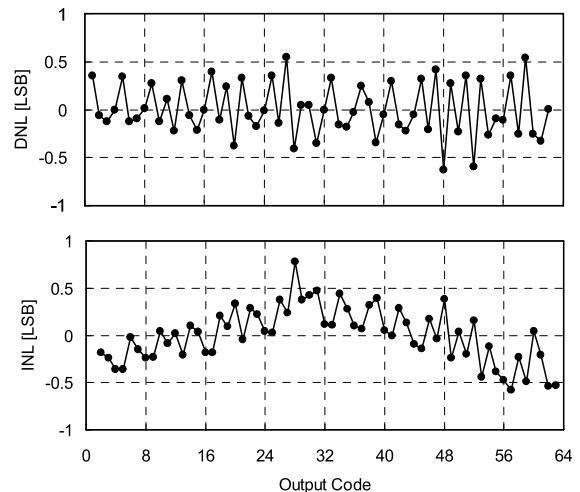

Fig. 24 Chip micrograph and layout.

Fig. 25 INL and DNL at 700 MS/s after CAL.

800 MS/s. Figure 27 shows the dependency of SNDR on the input frequency at 700 MS/s. The curve shows the SNDR of 34 dB (5.3 bit) is maintained up to the Nyquist input frequency of 350 MHz. The power dissipation is only 7 mW at the conversion rate of 700 MS/s. The figure of merit, as calculated with

$$FoM = \frac{P_d}{f_{sample} \cdot 2^{ENOB}} \qquad (15)$$
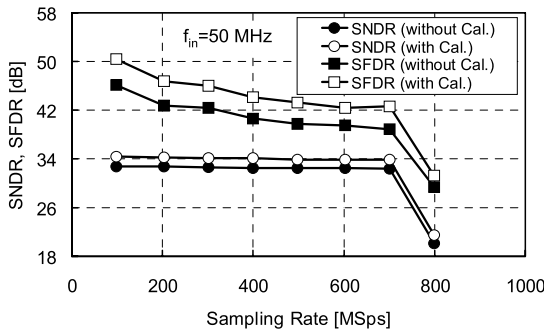
of 250 fJ/conversion steps.

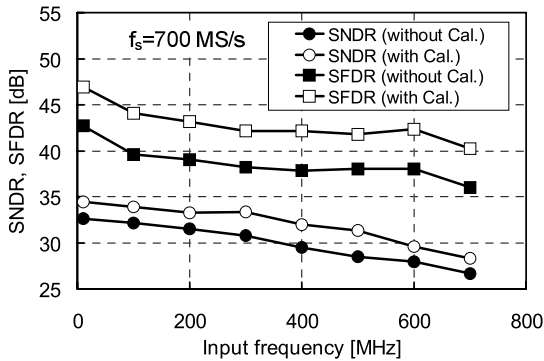**Fig. 26** SFDR and SNDR vs. sampling rate.

Fig. 27 SFDR and SNDR vs. input frequency.

Table 2 summarizes the ADC performance of this work and the recently published ADCs in the same resolution and similar target specification. As shown in Table 2, the proposed ADC consumes less power than other ADCs except [7] and [8]. [2] and [3] achieved high speed operation; however, they have large power dissipations due to use of the flash architecture. [17] also achieves high speed operation; however, the power dissipation is also large. [8] shows very impressive performance but 4 times interleaving makes the design difficult. [7] shows similar performance of the proposed ADC, however, it is necessary to examine the timing margin carefully because of the interleaving scheme.

5. Conclusion

We have demonstrated the subranging architecture using the CDAC, gate-weighted interpolation scheme and double-tail latched comparator with capacitive offset calibration. By introducing the CDAC, better performance of power dissipation, settling time and noise is achieved compared to the RDAC. A small area is also achieved by eliminating S/H circuit. A gate-weighted interpolation is implemented in the saturation region with sufficient performance for a 6-bit resolution ADC. This technique enables the realization of an interpolation in a simple way. Capacitive offset calibration reduces the comparator's offset dramatically from 10 mV to 1.5 mV per sigma. The fabricated ADC occupies 0.13 mm² die size and achieves 34 dB SNDR with Nyquist input frequency at 700 MS/s. The power dissipation is only 7 mW and the attained FoM is 250 fJ/conv.

Acknowledgments

Table 2 ADC performance summary.

Refer-ence	Process [nm]	Resolution [bits]	Sampling frequency [Gs/s]	Power dissipation [mW]	SNDR (DC/Nyq.) [dB]	FoM [pJ/conv.]	Active area [mm²]	Supply Voltage [V]	Architecture
[2]	90	6	3	90	37/ 34 (500 MHz)	4.6	0.28	1.2	Flash
[3]	45	6	1.2	28.5	36/34	0.45	0.1	1.2	Flash
[7]	65	6	1	6.27	31.5/28.5	0.21	0.11	1.2	SAR, Interleaving
[8]	40	6	2.2	2.6	31.6/29.6	0.04	0.03	1.1	Pipeline, Interleaving
[17]	90	6	2.7	50	36.5/33.6	0.47	0.36	1	Folding, Interleaving
This Work	90	6	0.7	7	35/34	0.25	0.13	1.2	Subranging

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Appendix A

Figure A·1 shows a CDAC which has the same structure with Fig. 18. V_{IN} and parasitic capacitor are ignored and one of the two reference voltages is changed to GND to simplify
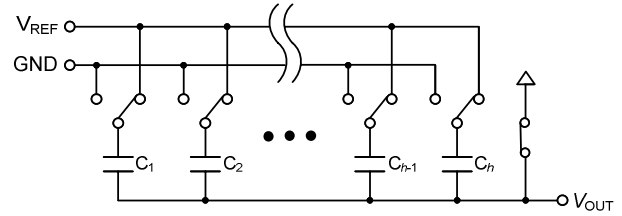

Fig. A·1　Simplified CDAC schematic.

the analysis. The number of capacitors in the CDAC, h, is decided by resolution of the CDAC. All of the capacitors in the CDAC have the same capacitance, it means $C_1 = C_2 = \ldots = C_h$.

When m-th capacitor changes its connection node, the variation of output voltage, V_{STEP} is represented as (A·1).

$$V_{STEP} = \frac{C_m}{\sum_{i=1}^{h} C_i} V_{REF} \tag{A·1}$$

A sensitivity of V_{STEP} by the variation of each capacitance is represented as below.

$$\Delta V_{STEP} = \frac{\partial V_{STEP}}{\partial C_1} \Delta C_1 + \frac{\partial V_{STEP}}{\partial C_2} \Delta C_2 + \cdots + \frac{\partial V_{STEP}}{\partial C_h} \Delta C_h \tag{A·2}$$

$$\Delta V_{STEP} = \left\{ -\frac{C_m}{\left(\sum_{i=1}^{h} C_i\right)^2} \left(\sum_{i=1}^{m-1} \Delta C_i + \sum_{i=m+1}^{h} \Delta C_i\right) \right. \\ \left. + \frac{\left(\sum_{i=1}^{m-1} C_i + \sum_{i=m+1}^{h} C_i\right)}{\left(\sum_{i=1}^{h} C_i\right)^2} \Delta C_m \right\} V_{REF} \tag{A·3}$$

Because all of the capacitors have the same capacitance, it is possible to substitute for all capacitors to C, (A·3) can be simplified as (A·4).

$$\Delta V_{STEP} = \frac{1}{(hC)^2} \left\{ -C\left(\sum_{i=1}^{h-1} \Delta C_i\right) + (h-1) C \Delta C_m \right\} V_{REF} \tag{A·4}$$

Equation (A·4) can be organized including standard deviation form, such as $\Delta C/C(\sigma)$.

$$\Delta V_{STEP}(\sigma) \\ = \frac{1}{h^2} \left\{ \sqrt{\left\{-\left(\sum_{i=1}^{h-1} \frac{\Delta C_i}{C}(\sigma)\right)\right\}^2 + \left\{(h-1) \frac{\Delta C}{C}(\sigma)\right\}^2} \right\} V_{REF} \tag{A·5}$$

In the (A·5), each $\Delta C_i/C(\sigma)$ has the same value because all capacitors have the same capacitance. Equation (A·5) is calculated as below.

$$\Delta V_{STEP}(\sigma) = \frac{1}{h^2} \sqrt{h(h-1)} \frac{\Delta C}{C}(\sigma) V_{REF} \tag{A·6}$$

To express (A·6) using total capacitance, C_{total}, $\Delta C_{\text{total}}/C_{\text{total}}(\sigma)$ is substituted for $\Delta C/C(\sigma)$.

$$\frac{\Delta C}{C}(\sigma) = \sqrt{h}\frac{\Delta C_{\text{total}}}{C_{\text{total}}}(\sigma) \qquad (A\cdot 7)$$

Substitute (A·7) to (A·6) and normalize to the LSB format of the ADC

$$DNL(\sigma)\,[\text{LSB}] = 2^N \frac{\Delta C_{\text{total}}}{C_{\text{total}}}(\sigma)\,\frac{1}{\sqrt{h}}\sqrt{1-\frac{1}{h}} \qquad (11)$$

where N is the resolution of the ADC.

Appendix B

The comparators in the proposed ADC calibrate its offset voltage by adjusting the slew rate of the input MOS transistor.

The slew rate is defined as (A·8)

$$SR = \frac{dV_{\text{OP\_1st}}}{dt} = \frac{I_P}{C_{\text{OP\_1st}}} \qquad (A\cdot 8)$$

where $V_{\text{OP\_1st}}$ and I_P are illustrated in Fig. 20. $C_{\text{OP\_1st}}$ means node capacitance including offset calibration capacitance in the $V_{\text{OP\_1st}}$. In this case, we explained using the positive side; however, it is also applicable to the negative side.

The current I_P flows through the input MOS transistor in the comparator. Therefore, it can be expressed as (A·9)

$$I_P = \alpha \cdot V_{eff}^2 \qquad (A\cdot 9)$$

where α means a coefficient and V_{eff} means V_{gs}-V_{th} of the input MOS transistor. Substitute the I_P in (A·9) to (A·8), the slew rate is derived as (A·10).

$$SR = \frac{\alpha \cdot V_{eff}^2}{C_{\text{OP\_1st}}} \qquad (A\cdot 10)$$

The main reason of the offset voltage of the comparator is the mismatch of the threshold voltage, especially the input MOS transistors. If there is an offset in the comparator, current I_P is changed; therefore, SR is also changed from its initial value.

According to (A·8), it is realized that the offset voltage can be described using V_{eff}, because V_{eff} includes V_{th}. The sensitivity of the offset by the variation of the calibration capacitance is expressed as (A·11).

$$\frac{\partial V_{off}}{\partial C_{\text{OP\_1st}}} = \frac{\partial V_{eff}}{\partial C_{\text{OP\_1st}}} = \frac{\partial SR/\partial C_{\text{OP\_1st}}}{\partial SR/\partial V_{eff}}$$
$$= -\frac{V_{eff}}{2C_{\text{OP\_1st}}} \qquad (A\cdot 11)$$

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